REMARKS

In the Office Action dated December 19, 2008, claims 1-2, 4-12, and 14-20 were pending. Claims 3 and 13 have been withdrawn from consideration. Claims 1, 5, 7, 8, 9, 10, 11, 15, 17, 18, 19 and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Dhir et al. (US 2005/0084076 A1), hereafter "*Dhir*". Claims 2, 4, 6, 12, 14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dhir in view of Lo (US 5,995,514), hereinafter "*Lo*".

Claims 1, 4, 5, 11, 14, and 15 are amended.

Claims 1, 5, 7, 8, 9, 10, 11, 15, 17, 18, 19 and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Dhir. Applicants respectfully traverse this rejection.

Furthermore, as regards independent claims 1 and 11, it was asserted that signal lines 106 in Dhir were analog circuitry as claimed. However, in Applicant's FIG. 3, signal lines 350 are distinct from analog circuitry 350. Signal lines are typically not analog circuitry, but rather merely wires. This element are missing from the Dhir reference.

Furthermore, it was asserted that Dhir showed digital circuitry coupled to analog circuitry in the MII 108 coupled to the signal lines 106. However, these claims have been amended to clarify that this coupling has to be direct, and in Dhir, the coupling is via PHY-1 102 and PHY-2 104, and therefore, they are not *directly* coupled. This element are missing from the Dhir reference.

Furthermore, it was asserted that Dhir provided a crypto communications module in the form of an encryption algorithm mod 305 in FIG. 6 coupled to the encryption

engine 112 (FIG. 1), 321 (FIG. 8). However, in the presently claimed invention, the crypto communications module 625 is separate from the crypto/ security logic 620 (FIGs. 6a-6e). Indeed, the reference in Dhir does not show a connection at all between the crypto engine and crypto communications module, since the former is shown in FIGs. 1 and 8, and the later in FIG. 6. Also note that the claims are amended to clarify that they are *directly* coupled. These elements are missing from the Dhir reference.

Furthermore, it was asserted that the PHY communications module was operatively coupled to the crypto communications module via program memory 301, 312. However, these claims are amended to clarify that the PHY communications module and the crypto communications module are operatively coupled via an interface link (FIGs. 6a-6e #630; [0054]). Program memory is not an interface link, as defined in Applicants' specification, nor are configuration logic blocks 307. No interface link between the PHY communications module and crypto communications module is shown. This element are missing from the Dhir reference.

For all these reasons, Applicants respectfully submit that a prima facie case of anticipation has not been made for these independent claims, that the rejection of these claims for this reason is therefore improper, and request that this rejection be withdrawn. The remaining claims are dependent upon these two independent claims, and should therefore be allowable for the same reasons.

Furthermore, as to claims 5 and 15, it was asserted that Dhir showed a master communications module coupled between the PHY communications module and the crypto communications module. First note that all three elements here, the master

communications module, the PHY communications module, and the cyrpto communications module are show in Dhir FIG. 1 as the MII module 108. However, this does not show that they are coupled (see argument for claims 1 and 11 above), just that they might exist. This is unsatisfactory in making a prima facie case of anticipation, since the claim claims the means for connecting the first two elements via the interface link. Furthermore, the claims are amended to clarify that the first two elements are directly coupled to the interface link. These elements are missing from the Dhir reference.

Since these claims are dependent upon independent claims 1 and 11 above, and for these additional reasons, applicants respectfully submit that a prima facie case of anticipation has not been shown, that the rejection of these claims as anticipated by Dhir is improper, and request that this rejection of these claims be withdrawn.

Claims 2, 4, 6, 12, 14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dhir in view of Lo. Applicants respectfully traverse this rejection. Furthermore, these claims are dependent upon independent claims 1 and 11, argued above, and should be allowable for the same reasons.

Furthermore, in regards to claims 2 and 12, Lo shows an interface between an MII (Dhir FIG. 1 #108) and MAC (FIG. 1 #110) (see Lo Abstract). However, the claim requires that the PHY (Dhir FIG. 1 #102, #104) be configured to provide connectivity through a MDIO/MDC interface, and the PHY controls operations of the crypto device. Thus, the claim requires that the PHY communicate utilizing the MDIO/MDC interface with the crypto device, but that interface is between the MII 108 and MAC 110 (Dhir

FIG. 1) according to Lo. This is not the same thing. This element is therefore missing from the combined reference.

Furthermore, in regards to claims 4 and 14, the claims are amended to clarify that the crypto communications module is *directly* coupled to the MDIO/MDC interface. This element is missing in the combined reference.

Therefore, for all of the above reasons, Applicants respectfully submit that a prima facie case of obviousness has not been made for these claims, that the rejection of these claims as obvious is improper, and request that this rejection be withdrawn.

Applicants believe that the above-identified application is now in condition for allowance and such action is respectfully requested.

If the Examiner has any questions regarding this application or this response, the Examiner is requested to telephone the undersigned at 775-586-9500.

Respectfully submitted,
SIERRA PATENT GROUP, LTD.

Dated: March 11, 2008

/bruce e. hayden/

Bruce E. Hayden
Reg. No.: 35,539

Sierra Patent Group, Ltd.
1663 Hwy 395, Suite 201
Minden, NV 89423
(775) 586-9500